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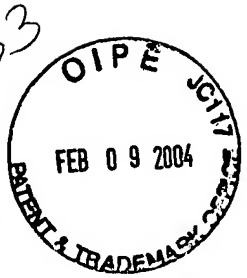


02-10-04.

AF/3729

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

IN RE: HUBER, Louis P., et al.)
)
SERIAL NO: 10/091,792)
) **APPEAL NO. _____**
FOR: METHOD FOR MANUFACTURING A POWER CHIP RESISTOR)
) **BRIEF ON APPEAL**
FILED: March 6, 2002)
)
GROUP ART UNIT: 3729)
)
ATTORNEY DOCKET NO. P04870US1)

To the Commissioner of Patents and Trademarks
Mail Code Appeal Brief - Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Dear Sirs:

Please enter the following Brief on Appeal into the record.

CERTIFICATE OF MAILING BY EXPRESS MAIL

I hereby certify that this document and the documents referred to as enclosed therein are being deposited with the U. S. Postal Service in an envelope as "Express Mail Post Office to Addressee" addressed to: Commissioner of Patents, Mail Stop Appeal Brief - Patents, P. O. Box 1450, Alexandria, VA 22313-1450, on 9th day of February, 2004.

John D. Goodhue

John D. Goodhue
Express Mail Label # EV 366850859 US

I. REAL PARTY OF INTEREST

According to MPEP § 1206, identification of the real party of interest will allow members of the board to comply with ethics regulations. This application has been assigned to Vishay Dale Electronics, Inc., a Delaware Corporation, having an address of 1122 23rd Street, P.O. Box 609, Columbus, NE, 68602-0609.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences at this time.

III. STATUS OF CLAIMS

Claims 33-37 are pending and appealed. No other claims are currently pending.

IV. STATUS OF AMENDMENTS

Applicant's Amendment After Final dated December 8, 2003, has been entered, as stated in the Examiner's Advisory Action dated December 22, 2003 (Paper No. 8).

V. SUMMARY OF INVENTION

The present invention is directed towards a method of manufacturing a stacked power chip resistor that increases the amount of heat dissipated without requiring additional board space. Separate chip resistors are stacked, with an inert encapsulant (such as glass) positioned between each chip resistor (Specification, p. 3, last paragraph). Each chip resistor

has its own substrate, resistive element, and first and second end caps. First and second barriers are used to mechanically connect the first and second chip resistors to provide long term mechanical stability without requiring epoxy or other adhesive (Specification, p. 5, third paragraph). Each chip resistor in the stack can be a standard sized chip resistor (Specification, p. 6, second full paragraph).

VI. ISSUES

A. Does the Examiner fail to reasonably interpret claims 33-37 by reading them so broadly as to cover a single chip resistor formed from a plurality of layers instead of two separate chip resistors, each with its own end caps, that are connected through use of metal barriers?

B. Does the Examiner fail to reasonably interpret claims 33-37 by reading them so broadly as to cover a single termination on each end of a chip resistor (a total of two structural elements) instead of two stacked chip resistors, each having its own end caps (four structural elements), and opposite barriers (two additional structural elements) for a total of six structural elements?

C. Does U.S. Patent No. 4,267,634 to Wellard disclose forming a stacked power chip resistor by "separating a first chip resistor from a second chip resistor with a glass encapsulant, each chip resistor comprising a substrate, a resistive element on the substrate and first and second end caps electrically connected to opposite ends of the resistive elements"?

D. Does U.S. Patent No. 4,267,634 to Wellard disclose a method of manufacturing a stacked power chip resistor that includes "connecting the first end cap of the first resistor and the first end cap of the second resistor with a first barrier to mechanically connect the first and second chip resistors" and "connecting second end cap of the first resistor and the second end cap of the second resistor with a second barrier to mechanically connect the first and second chip resistors to provide long term mechanical stability"?

VII. GROUPING OF CLAIMS

Claim 33 is an independent method claim from which claims 34-37 depend. Claim 33 has been rejected for anticipation by U.S. Patent No. 4,367,634 to Wellard. Claims 34-37 have been rejected for obviousness over Wellard. Therefore, it is submitted that Claims 33-37 rise or fall as a group.

VIII. ARGUMENT

It is well-settled patent law that in order to anticipate a claim under 35 U.S.C. § 102, a reference must disclose each and every element of the claim. See e.g. PPG Industries, Inc. v. Guardian Industries Corp., 75 F.3d 1558, 1566, 37 USPQ2d 1618, 1624 (Fed. Cir. 1996). Therefore, for Wellard to anticipate claim 33, Wellard must disclose each and every element of claim 33. The Examiner has failed to reasonably interpret the claims and has improperly relied upon Wellard.

A. The Examiner fails to reasonably interpret claim 33-37

1. The Examiner fail to reasonably interpret claims 33-37 by reading them so broadly as to cover a single chip resistor formed from a plurality of layers instead of two separate chip resistors, each with its own end caps, that are connected through use of separate and distinct barriers.

Claim 33 defines a stacked chip resistor from separate chip resistors (10). Note that claim 33 defines each constituent chip resistor (10) as comprising a substrate, a resistive element (12) on the substrate and first and second end caps (14) electrically connected to opposite ends of the resistive element (12). It is these chip resistors (10) that are stacked and each chip resistor (10) in the stack is electrically in parallel with the other chip resistors (10) in the stack. The barrier (18) connects the end caps (14) of each resistor. The barrier (18) provides for both electrical and mechanical connections of the chip resistors (10) within the stack. Due to this mechanical connection, adhesives or epoxy need not be used to connect the chip resistors (Specification, p. 5, third paragraph). The barrier also serves to absorb heat created through resistive heating (Specification, p. 5, fourth paragraph)... Also, due to this methodology, the chip resistors can be standard sized chip resistors that are stacked (Specification, p. 6, second full paragraph).

The Examiner has unreasonably construed claim 33. A first example of the Examiner's unreasonable construction is the manner in which the Examiner treats the limitations regarding "a first chip resistor" and "a second chip resistor." The structure of each of these constituent chip resistor is defined explicitly in claim 33 to include "a substrate, a resistive element on the substrate and first and second end caps electrically connected to

opposite ends of the resistive elements." Therefore, the only reasonable construction is that each chip resistor must include all of these elements.

Thus, it would be unreasonable to construe claim 33 to read upon a method of manufacturing a chip resistor formed through the stacking of layers, as opposed to the stacking of separate and discrete chip resistors, each chip resistor including its own substrate, resistive element, and first and second end caps. Although a stacking of layers may create a resistor, it does not create a "chip resistor" as is defined in the claims.

2. The Examiner fails to reasonably interpret claims 33-37 by reading them so broadly as to cover a single termination on each end of a chip resistor (a total of two structural elements) instead of two stacked chip resistors, each having its own end caps (four structural elements), and opposite barriers (two additional structural elements) for a total of six structural elements

In the Examiner's construction of claim 33, the Examiner does not require each chip resistor to have separate end caps (Office Action of November 14, 2003, Paper No. 6, p. 2-3, numbered paragraph 3). The Examiner does not require that the barriers be different structures from the end caps. (Office Action of November 14, 2003, Paper No. 6, p. 2-3, numbered paragraph 3). The Examiner's apparent position is that an end cap can be considered a termination means and therefore despite the claim calling for four separate end caps and two separate barriers, the claim is anticipated by two termination means. The Applicant does not dispute that an end cap can be used as a termination means (but not all termination means are end caps). Yet, the steps of claim 33 make clear that there are four

end caps (two end caps per constituent chip resistor) and two barriers (one on each end of the stacked chip resistor). Therefore, the only reasonable interpretation of claim 33 is that in order to meet the limitations of the claims, there must be four end caps and two barriers. Two termination means can not be considered to be four end caps and two barriers all at the same time

Claim 33 explicitly requires "separating a first chip resistor from a second chip resistor with a glass encapsulant." Claim 33 clearly requires "connecting the first end cap of the first resistor and the first end cap of the second resistor with a first barrier to mechanically connect the first and second chip resistors." Claim 33 explicitly requires "connecting the second end cap of the first resistor and the second end cap of the second resistor with a second barrier to mechanically connect the first and second chip resistors." Due to the interaction between these structures called for in the method claims, the Examiner's interpretation that allows the first end cap of the first resistor, the first end cap of the second resistor, and the first barrier to collectively be met by a single structure is not reasonable and in error.

B. U.S. Patent No. 4,267,634 to Wellard fails to anticipate as Wellard does not teach and every element of claim 33

1. Wellard does not disclose forming a stacked power chip resistor by "separating a first chip resistor from a second chip resistor with a glass encapsulant, each chip resistor comprising a substrate, a resistive element on the substrate and first and second end caps

electrically connected to opposite ends of the resistive elements", therefore Wellard does not anticipate

Wellard discloses a chip resistor, but the chip resistor of Wellard is not formed by stacking constituent chip resistors. Rather, Wellard uses a very different process to form a chip resistor. Wellard uses a layered approach where resistance or conductor patterns are sandwiched between ceramic materials (Abstract). After these layers have been formed, termination means 27 and 29 are secured to it in order to form a complete resistor chip (Col. 3, lines 43-54).

Claim 33 defines a stacked chip resistor formed from separate chip resistors (10). Note that claim 33 defines each constituent chip resistor (10) as comprising a substrate, a resistive element (12) on the substrate and first and second end caps (14) electrically connected to opposite ends of the resistive element (12). It is these chip resistors (10) that are stacked and each chip resistor (10) in the stack is electrically in parallel with the other chip resistors (10) in the stack. The barrier (18) connects the end caps (14) of each resistor. The barrier (18) provides for both electrical and mechanical connections of the chip resistors (10) within the stack.

Claim 33 expressly requires that the stacked chip resistor is formed from at least two separate chip resistors. Each constituent chip resistor is defined to include a substrate, a resistive element on the substrate and first and second end caps electrically connected to opposite ends of the resistive elements. This definition of a chip resistor is confirmed by

Wellard which states that "Once [sic] the chip 21 has had termination ends secured thereto, it is a complete resistor chip" (Col. 3, lines 53-55).

Wellard does not disclose forming a stacked chip resistor from constituent chip resistors. Figures 6 and 7 of Wellard indicate there is only one chip resistor 21 with termination means 29 and 27. Therefore the step of "separating a first chip resistor from a second chip resistor with a glass encapsulant" is not disclosed by Wellard. In Wellard, at best, it could be said that the layers within the chip resistor are separated. Yet this is not the same methodology as separating chip resistors where each chip resistor has its owns end caps. Therefore, Wellard can not anticipate.

2. Wellard does not disclose a method of manufacturing a stacked power chip resistor that includes "connecting the first end cap of the first resistor and the first end cap of the second resistor with a first barrier to mechanically connect the first and second chip resistors" and "connecting second end cap of the first resistor and the second end cap of the second resistor with a second barrier to mechanically connect the first and second chip resistors to provide long term mechanical stability", therefore Wellard does not anticipate

Wellard discloses a palladium-silver material which is deposited on the ends of a chip. Wellard describes this deposited material as "termination ends" (column 3, lines 50-54). In making the rejection based on Wellard, the Examiner apparently considers the termination means to be both end caps as well as a barrier. The Examiner says that elements 27 and 29 are end caps (Office Action of November 14, 2003, Paper No. 6, p. 2, numbered paragraph 3). The Examiner also says that elements 27 and 29 are metal barriers used for

connecting the end caps (Office Action of November 14, 2003, Paper No. 6, pp. 2-3, numbered paragraph 3). The Examiner can not have it both ways—particularly where the explicit steps of the claim require that these structures be treated as separate structural elements.

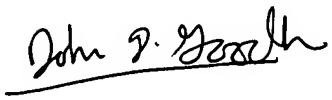
As previously explained, Wellard discloses two termination means, instead of the four end caps required by claim 33; as Wellard does not describe stacking separate stand alone chip resistors. The Examiner goes even further by equating the termination means 27 and 29 of Wellard to not only be the four end caps, but also to be the two barriers (18) on each end of the chips. The elements 27 and 29 cannot be both end caps and barriers. The structure of the device manufactured in claim 33 comprises four end caps and two barriers -- six separate structures. The Examiner is essentially triple counting the termination ends of Wellard. This should not be allowed. Moreover, the Examiner should not be permitted to count the termination means of Wellard as both end caps and barriers. It is clear that Wellard does not meet the limitations of claim 33. Therefore, Wellard does not anticipate.

VIIII. CONCLUSION

For the above-stated reasons, it is respectfully requested that the claims are in condition for allowability. The decision of the Examiner is without support, and unreasonably interprets the claims to eviscerate the very distinction that makes the art remote, and the invention patentability distinct. When the claims are interpreted as broadly as reasonable in light of the supporting disclose, Wellard does not anticipate.

Enclosed herein please find the Appeal Brief in triplicate. Please charge Deposit Account No. 26-0084 the required fee of $330.00.

Respectfully submitted,



JOHN D. GOODHUE, Reg. No. 47,603
McKEE, VOORHEES & SEASE
Attorneys of Record

801 Grand - Suite 3200
Des Moines, Iowa 50309-2721
515-288-3667 - mlw -